(12) UK Patent Application (19) GB (11) 2 168 533 A

(43) Application published 18 Jun 1986

(21) Application No 8530654

(22) Date of filing 12 Dec 1985

(30) Priority data
(31) 24125 (32) 18 Dec 1984 (33) IT

(51) INT CL⁴
H01L 23/50

(52) Domestic classification (Edition H):
H1K 5D9 5M2 PDX

(56) Documents cited
GB A 2088635 GB 1581285 EP A2 0086724

(58) Field of search
H1K
Selected US specifications from IPC sub-class H01L

(71) Applicant
SGS Microelettronica SpA (Italy),
Strada Primosole 50, Catania, Italy

(72) Inventor
Marzio Fusaroli

(74) Agent and/or Address for Service
Mewburn Ellis & Co,
2/3 Cursitor Street, London EC4A 1BQ

(54) Package for integrated circuits having improved heat sinking capabilities

(57) Increased heat dissipation is achieved by configuring enlarged metal areas (25") of the lead frame (23) of the package that are extensions of the portion (11) of the lead frame to which the integrated circuit chip is mounted in the assembly of the semiconductor package. The increased lead frame area provides increased contact with the package housing and provides a thermal conduction path in close proximity to the exterior surface of the package housing. The integrated circuit chip has a more efficient thermal path to the ambient air thermal heat sink.

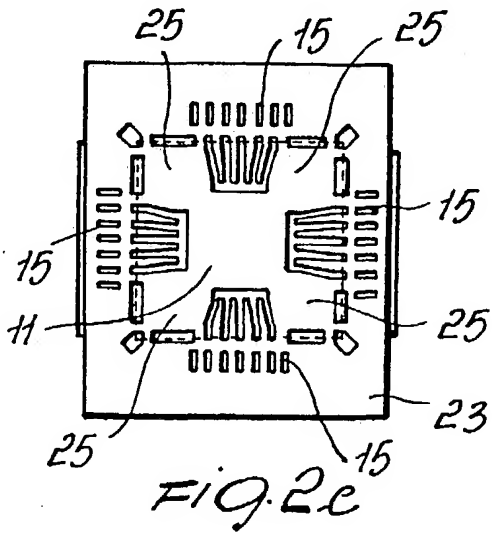

Fig. 2c

GB 2 168 533 A

2168533

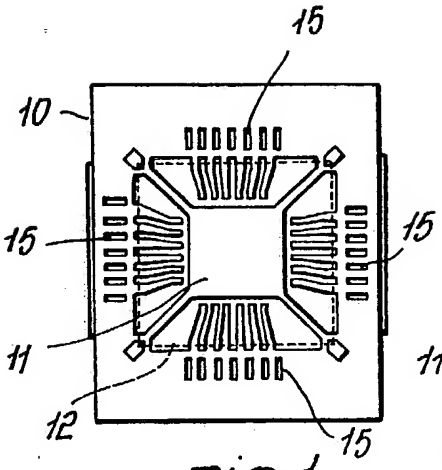

Fig.1

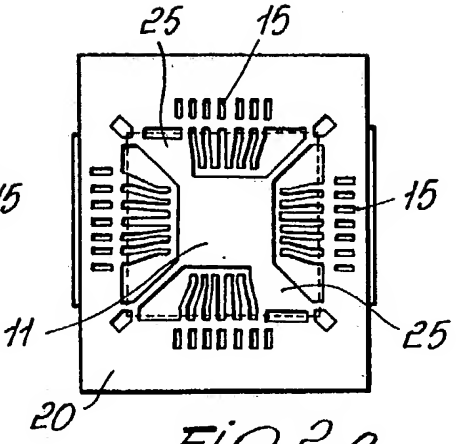

Fig.2a

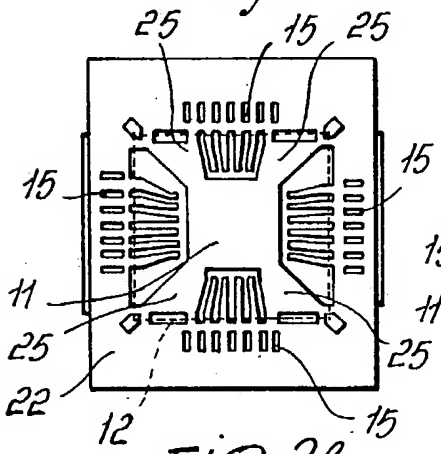

Fig.2b

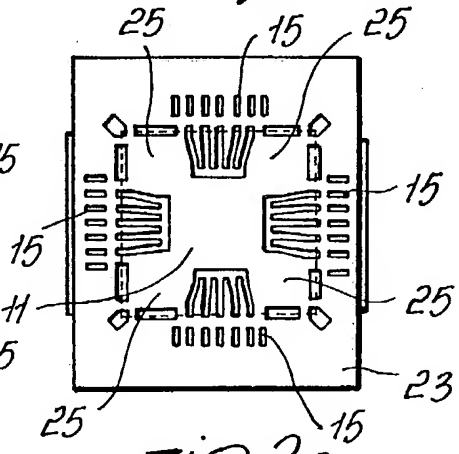

Fig.2c

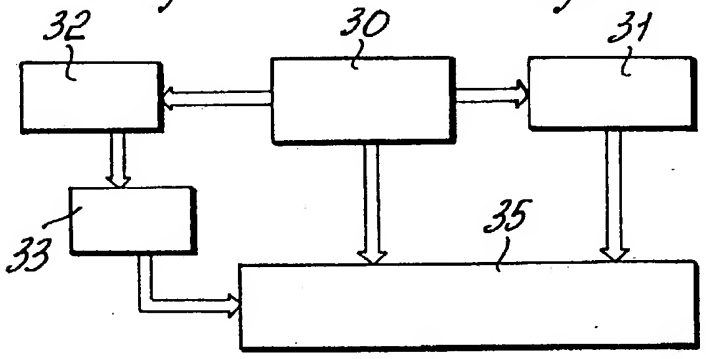

Fig.3

SPECIFICATION

Package for integrated circuits having improved heat sinking capabilities and method

This invention relates to a package for integrated circuits having improved heat sinking capabilities and to a method for increasing heat dissipation.

As the density of elements formed on a substrate of an integrated circuit configuration has increased, the problem of dissipation of heat generated therefrom has become increasingly important. If heat is not dissipated, the resulting rise in temperature of the entire integrated circuit and package can have a deleterious effect on the operating characteristics of the integrated circuit. Heat sinks can be thermally coupled to semiconductor component housing packages to assist in the removal of the heat. However, the integrated circuit housing package is typically a poor thermal conductor, so this technique has been of limited value.

Other techniques for attempting to cool the chip by heat sinking have included adding a cooling plate in contact with the integrated circuit. However, the cooling plate, an effective solution to the heat dissipation, results in problems that involve the use of special circuit boards to accommodate the cooling plate.

Therefore, a need exists for an improved cooling technique that can be implemented using the present packaging methods and would result in improved heat dissipation through the integrated circuit package without special adapting devices in the electronic circuit.

It is therefore an object of the present invention to provide an improved package for dissipating heat generated in an integrated circuit chip.

It is another object of the present invention to provide an improved package for conducting heat generated in an integrated circuit chip that can be implemented with current packaging techniques.

Yet another object of the present invention is to provide a method for improving the thermal conduction connection between an integrated circuit chip and a housing package to which the chip is mounted.

The aforementioned and other objects are accomplished, according to the present invention, by providing a lead frame geometry having additional thermal mass for increasing the thermal inertia while providing additional thermal paths for conduction of heat away from the integrated circuit chip.

In accordance with the present invention, a package for semiconductor circuits is disclosed, including a semiconductor chip, a lead frame having regions for electrical coupling to the semiconductor chip, the lead frame including a flag region and an enlarged associated area mechanically coupled to the semiconductor chip, and a housing package for enclosing the integrated circuit chip and at least preselected portions of the lead frame.

Moreover, in accordance with the present invention, a method is disclosed for increasing the cooling of an integrated circuit chip in a package housing, comprising the step of enlarging an area of a lead frame coupled to said integrated circuit chip.

These and other features of the invention will be understood by reading the following description along with the figures.

Figure 1 is a top view of a typical lead frame geometry;

Figures 2a, 2b and 2c are top views of examples of lead frame geometry for improved semiconductor chip heat dissipation according to the instant invention; and

Figure 3 is a diagram of the flow of heat between the integrated circuit chip and the housing package.

Referring to Fig. 1, Fig. 2a, Fig. 2b and Fig. 2c, a plurality of lead frame configurations 10,20,22 and 23 are shown. Interior section 11 of each configuration is made of suitable metal and is usually silver plated and is referred to as the flag area of the lead frame. Isolated from but surrounding the metallic region or flag area 11 about the four sides thereof are a plurality of leads 15. In assembly, an integrated circuit chip is bounded or mounted to flag area 11, as is understood, with leads 15 being electrically connected to the chip by wire bonding, for example. Dotted line 12 indicates the general area that the package housing occupies. The interior of the region indicated by the dotted lines can be filled with a plastic or resin material that will serve as structural support for the elements of the package, including the wires coupling the integrated chip and the conducting leads 15 of the lead frame. A cap encloses the housing to environmentally seal the package. In Figs. 2a, 2b and 2c, areas 25,25',25" indicate regions that normally do not include a significant amount of lead frame structure.

Referring now to Fig. 3, the flow of heat from the integrated circuit chip to the exterior of the package housing is shown schematically. Integrated circuit chip 30 is the source of the heat. The chip 30 is seated on flag 11 and through this flag (flag 31 in Fig. 3) transfers heat to the package housing 35. In addition, heat from chip 30 is transferred directly to the package housing 35. Heat can also be transferred via wires 32 to leads 33 (corresponding to leads 15) and to package housing 35.

The heat generated by the semiconductor chip can be conducted to the exterior surface of the package housing by a plurality of paths. The increased areas 25,25',25" of the lead frame coupled to the flag area 11 can assist in flow of heat to this surface. First, the

added mass provides for temperatur inertia. Next, the lead frame, being fabricated of a relative good thermal conductor, provides an increased area for contact with the housing package permitting a more uniform transfer of heat. Finally, the enlarged conducting areas of the lead frame are relatively close to the surface of the package housing. In typical electronic circuits employing integrated circuit packages, the typical heat sink is the air surrounding the package. The package, being comprised of a relatively poor thermal conductor can provide better cooling of the interior integrated chip when the heat can be distributed in close proximity to the package exterior.

Referring once again to Fig. 3, the increased area of the lead frames enlarges the thermal path from the chip 30 to the flag 31 and to the housing.

As shown in Fig. 2a, the lead frame 20 comprises two enlarged metal areas 25 that are joined in opposite corners of the lead frame. Similarly, lead frame 22 has four enlarged metal corner areas 25' mechanically and thermally connected to flag area 11. These enlarged corner metal areas 25 increase the heat dissipating characteristics of flag area 11 to which the semiconductor integrated circuit chip is mounted.

It will be clear by reference to Fig. 2c that the increased heat dissipation provided by the enlarged thermal conducting area 25" of the lead frame 23 is obtained at the expense of fewer leads to the external circuit board.

This description is meant to describe the preferred embodiment and is not meant to limit the scope of the invention. The scope of the invention is to be limited only by the following claims. Many variations will be apparent to one skilled in the art that would yet be encompassed by the spirit and scope of the invention.

CLAIMS

1. A package for semiconductor circuits comprising a semiconductor chip; a lead frame having metal regions electrically coupled to said semiconductor chip; said lead frame having a flag region mechanically coupled to said semiconductor chip; and a housing package for enclosing said semiconductor chip and at least selected portions of said lead frame, characterized in that interior portions of said lead frame mechanically coupled to said flag region and said semiconductor chip have an increased area.

2. The package of Claim 1, characterized in that said increased lead frame porti ns are in corners of said housing package.

3. A lead frame for providing increased dissipation of heat generated in a s miconductor chip mounted to the l ad frame, comprising a center metallic flag r gion and a plurality of metallic leads extending outwardly from said flag portion, said leads surrounding said flag region and being isolated therefrom, characterized by enlarged metal areas formed in at least two corners of the lead frame opposite one another between adjacent sets of said plurality of leads that are transverse to one another, said enlarged metal areas being mechanically and thermally connected to said flag region.

4. The lead frame of Claim 3, characterized in that it includes two additional enlarged metal areas mechanically and thermally connected with said flag region, said two additional metal areas being formed in the remaining opposite corners of the lead frame.

5. The method of increasing the dissipation of heat generated in an integrated circuit chip to be mounted in a package, characterized by the step of enlarging the corner area of the flag area of the lead frame assembly of the package mounted to said integrated circuit chip.

Printed in the United Kingdom for
Her Majesty's Stationery Office, Dd 8818935, 1986, 4235.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.